Cointegration of Optoelectronics and Submicron CMOS

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Abstract

The rapid emergence of multi-chip modules (MCMs) and the continuing interest in wafer scale integration (WSI) provide important opportunities for successful insertion of high performance optical interconnections into real systems. The large area substrates and the distances between packaged wafer-level modules introduce distances of sufficient length that propagation of very high speed digital signals along electrical lines will be difficult. At the same time, the substrates allow use of thin film technologies for fabrication of optoelectronic devices, optical waveguides and other optical elements, drawing on the natural alignment accuracy of photolithographic definition of optical components to avoid several practical problems arising when optical elements are surface mounted. For such reasons, large area silicon wafers provide an important potential application for more aggressive use of optical interconnections. This paper addresses two specific issues impacting the eventual application of optical interconnection in such full-wafer systems. The first issue is growth of GaAs semiconductor regions within a silicon WSI or MCM substrate containing high performance silicon CMOS circuitry, seeking to cointegrate optical and silicon VLSI devices. The second concerns addition of VLSI electronics to provide an "intelligent" detector array which can electronically establish alignment with an incident bundle of optical beams. These issues are considered from the perspective of massively parallel optical interconnections between packaged wafer-level components.

I. INTRODUCTION

Multichip modules (MCMs) provide an advanced, electrical interconnection technology which avoids several traditional performance limits imposed by packages holding individual integrated circuits (ICs). Although the individual packages of ICs are eliminated within the MCM, the MCM itself must be packaged and packaging limits equal to or more severe than those of individually packaged ICs reappear. Direct, free-space optical interconnections between adjacent MCMs are an attractive, longer term approach for massively parallel interconnections between MCMs. However, such optical interconnections introduce several critical technology issues. Two such issues are considered here – in particular (1) the cointegration of III-V optical sources with silicon VLSI control/driver circuitry and (2) the cointegration of silicon VLSI control electronics with optical detectors (silicon or III-V semiconductors) to provide "electronic" alignment rather than mechanical alignment.

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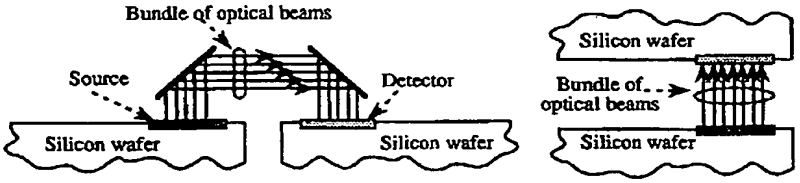

Figure 1: Massively parallel optical interconnections between source and detector arrays on silicon substrates (MCMs or WSI).

A wide variety of optical systems have been developed or suggested in the general area of optical computing and optical interconnects to direct and focus a dense array of optical beams on some target region [1]–[11]. The specific optical system directing a bundle of optical beams from an optical source array (e.g. array of semiconductor lasers) on one MCM to an optical detector array on another array is not considered here. Instead, the source and detector arrays are emphasized. Figure 1 illustrates the basic source array and detector array configurations (ignoring the optical system connecting them) for connections between horizontally adjacent or vertically adjacent MCMs.

If there are only a few optical sources (detectors) on each array, then hybrid mounting of the array on the MCM is a reasonable approach. However, a large number of sources (detectors) on each array IC requires a correspondingly large number of electrical inputs (outputs) to the array. For massively parallel optical interconnections, hybrid mounting becomes unrealistic. A more promising approach is to directly integrate the source and detector arrays within the MCM substrate. Below, MCMs using silicon substrates or WSI silicon circuits are assumed with this objective in mind.

Monolithic integration of optical sources within a silicon substrate can draw on the extensive research and development work on heteroepitaxial growth of III-V semiconductors on silicon. Addition of fault tolerance to reconfigure an optical source array, avoiding defective sources, will favor the combination of silicon control circuitry with the optical sources. For this and other reasons, we are studying the compatibility of heteroepitaxial growth of GaAs-on-Si with commercial, submicron silicon CMOS devices, as discussed in Section II.

Next considered is addition of control electronics to a detector array to provide an electronic alignment of the overall detector array to an incident bundle of optical beams. Without such electronic alignment (a specialized form of array reconfiguration), MCMs would require precise mechanical positioning relative to one another to support massively parallel, free space optical interconnections among them. A new approach for "virtual alignment" in a recently initiated research project is presented in Section III.

II. COMPATIBILITY OF GaAs DEVICES WITH Si CMOS

III-V heteroepitaxial growth of GaAs devices on silicon wafers containing conservatively designed silicon MOSFETs has been demonstrated [12,13,14] but compatibility with deep submicron, commercial Si CMOS technologies remains suspect. Preliminary results from an ongoing study of compatibility of small area, GaAs growth with 0.9 μm CMOS are presented here.

The 4% lattice mismatch and 200% thermal expansion coefficient mismatch between Si and GaAs ensure that stresses will be present in GaAs films epitaxially grown on Si. Defect densities for GaAs-on-Si are typically in the range $10^7 \rightarrow 10^9\ cm^{-2}$, far

Thermal Step	Description	Temp (°C)	Time (minutes)	Atmosphere
1	Desorption	850-950	15-30	$H_2 + AsH_3$
	Reconstruction	950-1050	15-30	$H_2 + AsH_3$
2	Buffer Layer	300-400	5-10	MBE: vacuum MOCVD: $AsH_3 + TMG$
3	Anneal	750	10	As
4	SLS Filter	750	few	
5	MBE Cap Layer	700-750	120	vacuum
	MOCVD Cap Layer	700-750	120	$AsH_3 + TMG$
6	Normal Anneal	750-950	15	As
	Thermal Cycle	900/100	few	As
	Cavity Anneal	800-950	few	As

Table 1: Representative growth conditions for GaAs heteroepitaxy.

greater than the $10^2 \rightarrow 10^3\ cm^{-2}$ defect densities in GaAs starting wafers and in GaAs epitaxial layers on GaAs substrates. Further reduction of defect densities in GaAs-on-Si remains a critical issue, motivating a variety of specialized growth conditions (e.g. [15,16,17,18]) and constraining relaxation of GaAs heteroepitaxial growth conditions for compatibility with submicron Si CMOS.

Table 1 summarizes typical GaAs-on-Si growth conditions. The basic steps are as follows.

Step 1 – Si Surface Preparation: To avoid gross defects, removal (desorption) of the native oxide before GaAs growth is essential. In addition, the surface of the starting wafer typically is offset at a slight ($2 \rightarrow 4^o$) angle to provide surface structure (steps) which define the initial orientation of GaAs crystallites. Formation of the steps requires a high temperature surface reconstruction step.

Step 2 – Buffer Layer: Next, a thin buffer layer is grown slowly at low temperatures, providing a low defect density surface on which a thicker (i.e. *cap*) layer is grown more rapidly using higher temperatures.

Step 3 – Buffer Layer Anneal: A few reports favor annealing of the buffer layer before overgrowth of the capping layer.

Step 4 – SLS Dislocation Filters: Strained layer superlattices (SLS's) restrict the vertical propagation of dislocations into the overlaying cap layer and are favored by several workers.

Step 5 – Cap Layer Growth: The thick (few μm) cap layer is grown at higher temperatures than the buffer layer. In Table 1, a growth rate of 2 μm/hr and a film thickness of 4 μm is assumed, requiring about 2 hours for completion of the cap layer.

Step 6 – Final Anneal: A final *post-growth* anneal to reduce defect densities is used by several investigators.

The oxide desorption and surface reconstruction step is a concern for Si CMOS devices due to its high temperature while the cap layer growth step is a concern due to its long growth time.

Our studies have used silicon wafers processed by AT&T Microelectronics on their 0.9 micron, Twin-Tub CMOS fabrication line. To compare changes in the characteristics of devices and structures on different wafers, subjected to different conditions, all wafers were cut from the same ingot. Similarly, all wafers were processed as a single lot through the process line. One set of Si test wafers (with 0, 2, 4 and 6 degree surface misorientations) was processed normally. Just prior to metalization, a second set (also

with 0, 2, 4, and 6 degree surface misorientations) received additional thermal cycling[1] simulating GaAs heteroepitaxial growth conditions. The two sets were recombined for final metalization.

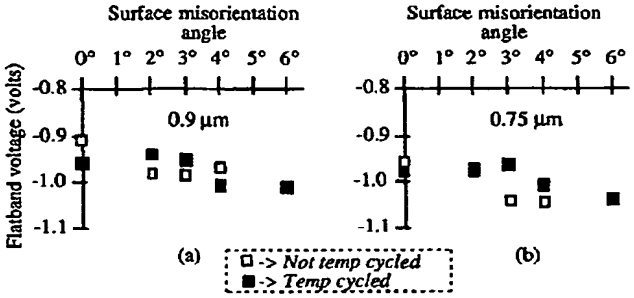

Figure 2: Flatband voltage for 0.9 μm and 0.75 μm n-channel MOSFETS with and without added temperature cycle

SPICE parameters for the BSIM short channel MOSFET model were obtained from device measurements using the BSIM2 parameter extraction software from the University of California at Berkeley. Only the threshold voltage V_{th} and low field mobility μ_0 results are considered here, though a full set of SPICE parameters are provided by the extraction. Device orientations are such that current flow was in the direction normal to the surface steps on the Si wafer.

The flatband voltage (which is a direct measure of the threshold voltage) is shown in Figure 2 for 0.9 μm and 0.75 μm n-channel MOSFETs (one device per point). A significant decrease in flatband voltage is seen for the larger surface misorientation angles, both for samples receiving the added temperature cycles simulating GaAs growth and for the normally processed samples. Evaluations of a larger number of devices will be needed to determine whether the flatband voltage shift is systematic (in which case the doping can perhaps be adapted to correct the shift) or whether there is an increased flatband voltage uncertainty as the misorientation angle increases.

Similar to the results in [19], we find an approximately 20% decrease in the low field mobility as the surface misorientation increases from 0 to 6° for both 0.9 μm and 0.75 μm n-channel MOSFETS and for both the normally processed devices and for devices receiving additional heat cycles.

A very pronounced effect of surface misorientation was observed in the source-to-substrate leakage current. Figure 3 shows the leakage current (combined source and drain to substrate leakage, though the source contribution dominates) as a function of reverse bias and as a function of misorientation angle for 20 μm n-channel MOSFETs processed normally. The 3° tilted devices showed a dramatic increase, relative to other tilt angles. Heat treated devices exhibited an large increase in leakage current for all angles. The cause of this increase in leakage current is under investigation.

Oxide wearout occurs when some total charge Q_t has passed through the oxide, at which time the gate oxide breaks down. The relation between time to breakdown of the oxide and the total charge Q_t is a result of the formation of trapped charge in the oxide, that trapped charge leading to higher, local electric fields eventually exceeding

[1]The maximum thermal cycling temperature was limited to 800° due to CMOS materials limitations set by the reflow glass layer.

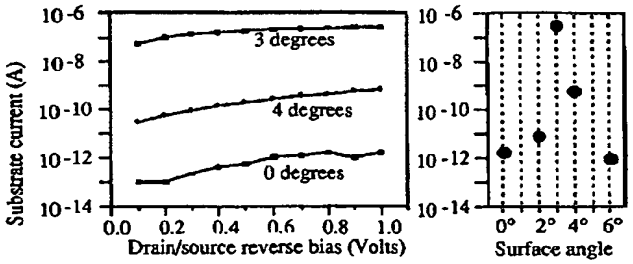

Figure 3: Source-to-substrate leakage current

the breakdown field of the oxide. Devices with lower charge to breakdown correspond to gate oxides with higher initial or more rapidly developing trapped charge or with lower oxide breakdown fields. Significant degradations in oxide wearout were observed in [19] with increasing surface misorientation angle and similar results were found here. Gate oxide wearout measurements were completed using a variety of standard techniques. Figure 4 shows the average charge to breakdown using a constant current stress measurement on capacitors corresponding to n-channel MOSFET gate regions for both normally processed samples and samples receiving the additional temperature cycles.

There is a considerable statistical spread in the charge to breakdown of otherwise identical devices due to localized weak regions in the oxide. Measurements on a larger sample size will be needed to obtain definitive results. The devices receiving additional thermal cycles display a smoother decrease in charge to breakdown in Figure 4 than those processed normally, suggesting a partial annealing of the weak oxide regions in the former samples.

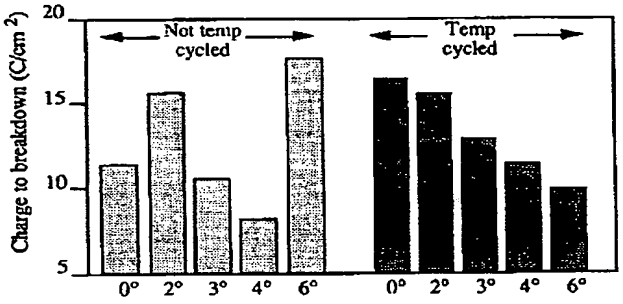

Figure 4: Charge to breakdown for capacitors representing the gate regions of n-channel device.

Overall, the thermal cycling and the surface misorientation impact several standard MOSFET parameters. The maximum temperature during the thermal cycling was considerably below the standard temperatures used for surface reconstruction/cleaning[2].

[2]Another set of wafers is presently being obtained to extend the temperature.

In addition, a variety of other degradation mechanisms (contact resistance, salicide integrity, etc.) remain to be evaluated. If the impact of GaAs heteroepitaxial growth on submicron CMOS continues to be modest, then the main barrier to cointegration of GaAs and Si VLSI will be cost. However, the effects seen here are sufficiently large that possible compatibility problems for deep submicron CMOS remain a serious concern.

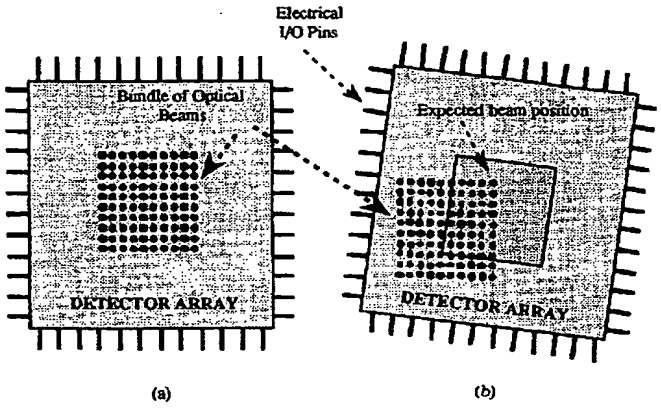

Figure 5: Detector array large relative to incident array of optical beams to handle misalignment. (a) Ideal aligoment. (b) Example of misaligned detector array.

III. VIRTUAL ALIGNMENT OF FREE SPACE OPTICAL INTERCONNECTIONS

Here, we consider a parallel "bundle" of optical beams incident on a detector array. Alignment errors occur in the position of the detector array during assembly of the system and as a result of thermal expansions of components relative to one another. Large area detectors could relax alignment tolerances but would also seriously reduce the density of optical interconnections. As suggested in Figure 5, small detectors can perhaps be retained despite alignment errors by using an oversized detector array, sufficiently large to accommodate alignment errors in the placement of the detector array. Such an array would require control circuitry within the array to extract the received digital signal from the array. Such an "intelligent" detector array would provide output data signals which are robust against alignment errors. The discussion below summarizes the design principles of the intelligent detector array. These are preliminary design guidelines, providing a general view of the issues involved.

Figure 6a illustrates external interconnections, to an $N \times N$ detector array. Signals from internal cells are routed to edge connections using the pie-cuts shown. Each edge connection is assigned to a boundary cell (for reasons given below), giving the "edge" I/O ports shown in Figure 6b. Each edge ports provides external connections not only to the boundary cells but also to the interior cells (i.e. the N^2 cells of the array must connect to $4(N-1)$ boundary ports). Figure 6c illustrates an example of routing of wires from the boundary of the array to the array cells. Each "interconnection" shown in Figure 6 represents three physical lines (signal, power, and ground).

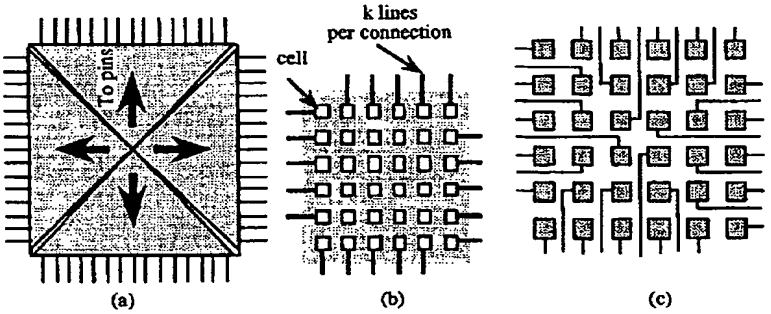

Figure 6: External connections to cells of detector array. (a) triangular regions feeding edges. (b) Assumed connections (with single connections to corner cells). (c) Example of layout of interconnections.

Wires to internal cells pass through the boundary cells and add to their area. A uniform distribution of detectors is assumed throughout the array and the area of the interior cells are equal to the area of the boundary cells. If a boundary cell handles connections to k cells of the array, the maximum size of the overall array is $N_{max} = 2k\left\lfloor 1 + \sqrt{1 - 1/k} \right\rfloor$. To obtain an array with $N > N_{max}$, the overall array must be divided into a set of subarrays, each subarray providing a uniform distribution of detectors and the subarrays separated by wiring channels (devoid of detectors).

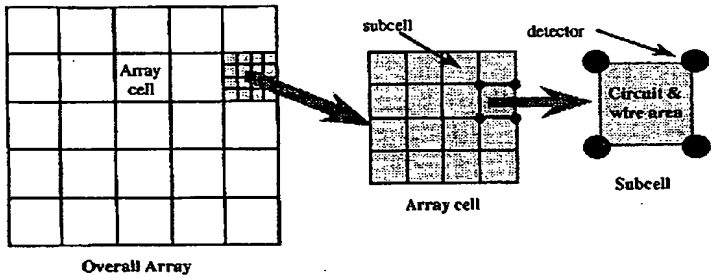

Figure 7: Hierarchical organization of detectors and associated electronics. (a) Array of cells, each cell detecting a single incident beam. (b) Array of subcells forming a cell. (c) Position of detectors in subcell.

Each of the cells in Figure 6 is itself an $m \times m$ array of subcells, each subcell a 2×2 of detectors as shown for $m = 4$ in Figure 7. The incident beam width is sufficiently large (1) to ensure that at least one detectors of a subcell is activated regardless of misalignment errors (within bounds on those errors noted earlier) and (2) the maximum number of detectors covered by a given incident beam is 4.

Figures 8 a and b illustrate two approaches for assignment of subcell electronics to detect the incident optical power. The two distinct cases correspond to (a) each

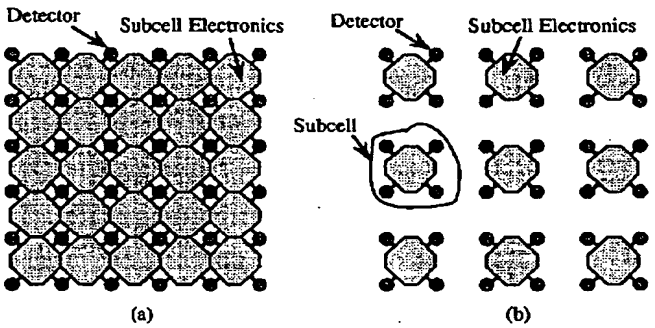

Figure 8: Two associations of electronics with detectors. (a) Each detector associated with 4 neighboring subcell electronics circuits. (b) Each detector associated with a single subcell electronics circuit.

detector of a cell associated electrically with four 2×2 neighboring subcells, except at the array boundary and (b) each detector associated electrically with only a single subcell. Here, only the former case is considered. The area of the 2×2 subcell corresponding to Figure 8c depends on (1) the area of the individual detectors (i.e. $(2r_d)^2$ where r_d is the radius a single detector, (2) any additional area around the detector for isolation, (3) the area for wires crossing through the cell, and (4) the area (A_{cir}) for electronic circuitry (both analog and digital electronics) associated with each cell.

The maximum efficiency of a detector (assuming the detector is covered by the optical beam) defines the efficiency of the overall cell, i.e. $\epsilon_{cell} \leq \epsilon_{det}(r_d^2/R_{beam}^2)$. Here, $R_{beam} = \sqrt{2}D$ (D the center-to-center spacing of detectors) is the minimum radius of the beam, ϵ_{det} is the efficiency of an individual detector relative to the optical power which is incident on the detector. Excessive wire area and electronic circuitry decreases the area available for the detector and thereby degrades the effective detector efficiency through the geometrical factor $(r_d/R_{beam})^2$.

The analog circuitry associated with each 2×2 subcell is roughly illustrated in Figure 9a. The output currents of the four detectors are combined in an analog circuit which fires when the total current exceeds some threshold. This provides a consistent response in the extreme cases of only a single detector illuminated and all four detectors illuminated. The response of the thresholding circuit is then amplified to produce a logic-level voltage signal.

The digital logic circuitry, illustrated schematically in Figure 9b, performs two major functions, one associated with the overall cell and the other handling boundaries between cells. The logic circuitry associated with a single cell combines the separate responses from the various subcells of that cell of the array to generate an output signal defining whether a beam is activating one of more detectors of the cell. More than one subcell of the cell can be active, as shown in Figure 7b. The logic circuitry associated with the boundary between cells is not well defined at this time.

IV. SUMMARY

Addition of GaAs to Si VLSI for parallel optical interconnects between MCMs confronts a number of compatibility issues to preserve the performance of the Si VLSI.

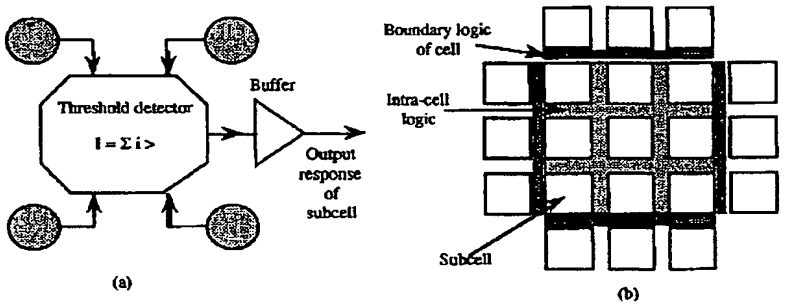

Figure 9: Illustration of (a) analog circuitry associated with a subcell and (b) digital logic circuitry associated with cell and cell boundaries

Continuing evaluations will be necessary to define the compatibility barriers. At the same time, addition of intelligent electronics can relax practical barriers to optical interconnects, as suggested here for "virtually aligned" optical detector arrays.

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